TinyCPU

4位微处理器设计

组员

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项目说明

Design Goal：

设计一个微型的CPU，包含运算器、控制器、寄存器、总线接口逻辑。

Software：

Xilinx ISE

Requirement：

VHDL

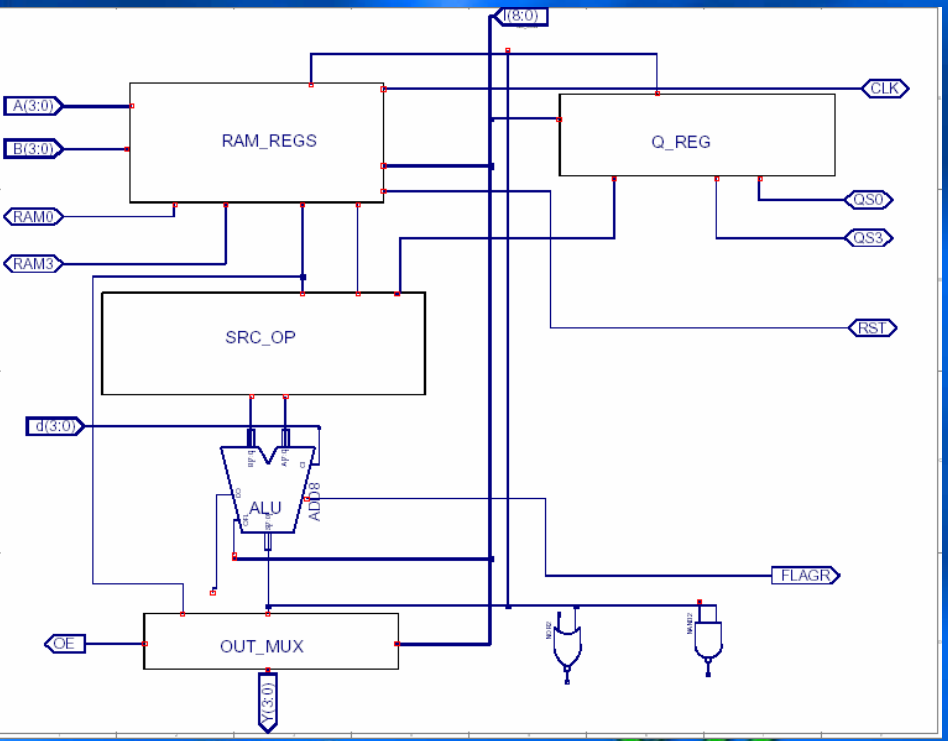
Idea I

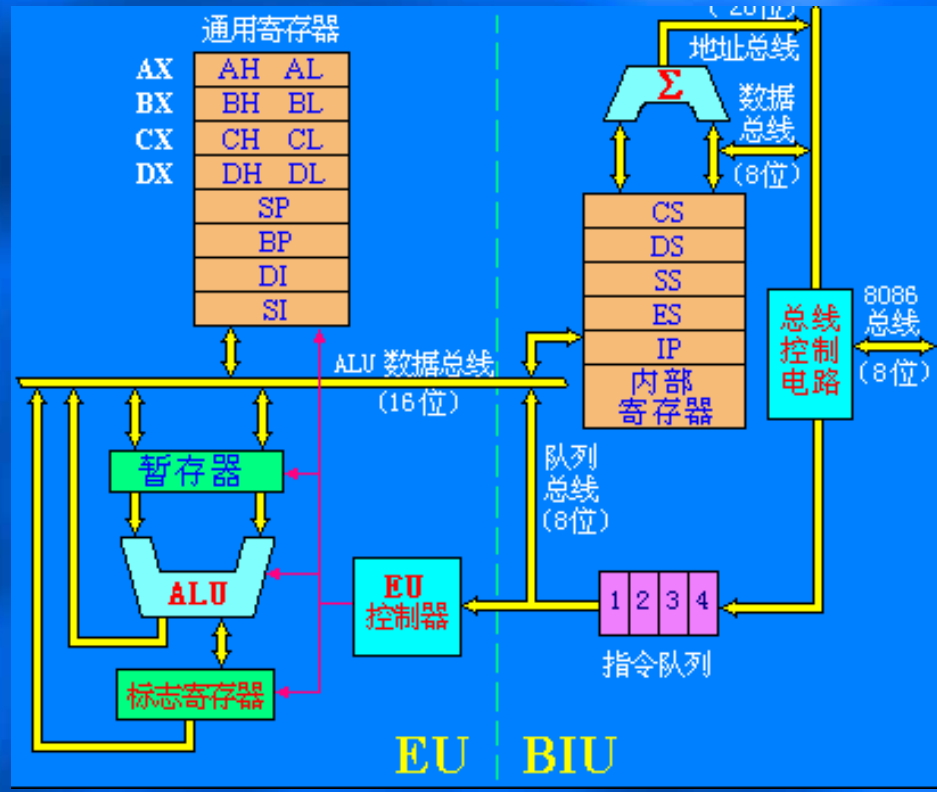
使用VHDL语言对一个复杂的电子实体设计，一般会采用自顶向下和自底向上两种不同的方式来完成。

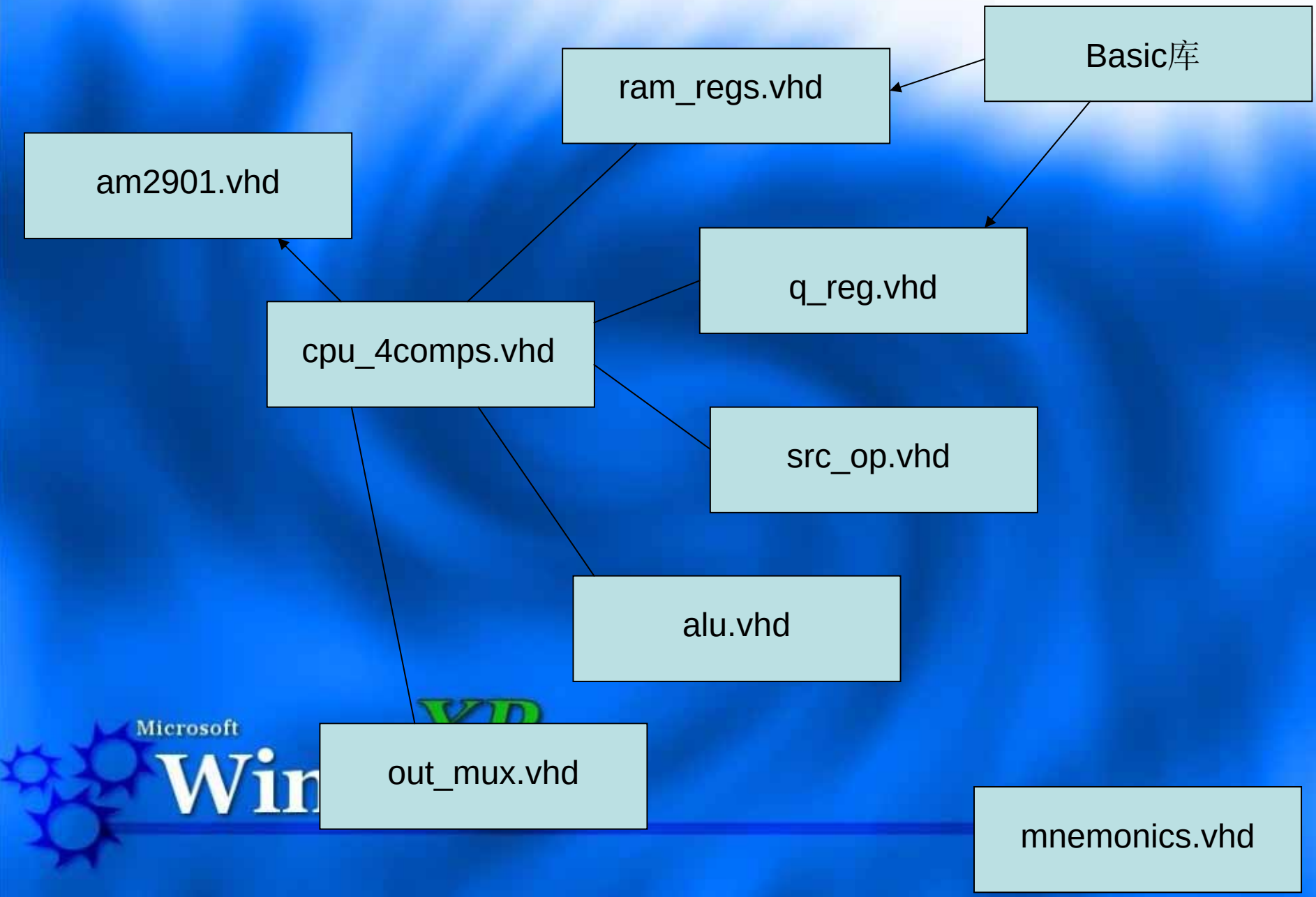
先从（其实也不是最低层开始，是从中层开始）该CPU的基本部件如ALU、通用寄存器、缓冲、选择控制、随机存储（暂存）开始完成。在完成的过程中，逐渐完成BASIC库（包括九种常用模块描述，并由regs_pkg.vhd打包描述）的建立，完成CPU组成部件后，对这五部分进行打包描述（在work中cpu_4comps.vhd中集合描述）。

Idea II

在完成最上层的描述，在最上层的结构体中完成对包中各模块的引用。此外，在work中还建立了一个微指令代码编程包，将该微处理器的指令代码规定其中。






Basic库
ram_regs.vhd
am2901.vhd
q_reg.vhd
cpu_4comps.vhd
src_op.vhd
alu.vhd
out_mux.vhd
mnemonics.vhd

OUT_MUX.vhd

- OUT_MUX.vhd微指令控制的2选1多路器由允许输出线oe和三态门y组成,可选4位数据f或ad输出到外围;

- port(
- ad,f: in std_logic_vector(3 downto 0);
- dest_ctl:in std_logic_vector(2 downto 0);
- oe: in std_logic;
- y: buffer std_logic_vector(3 downto 0));

- Architecture out_mux of out_mux is
- Signal y_int: std_logic_vector(3 downto 0);

Begin

- Y_int <=ad when dest_ctl=rama else f;
- --在控制下选择ad、f
- Y <= y_int when oe='0' else "ZZZZ"; --高阻态
- End out_mux;

ALU.vhd

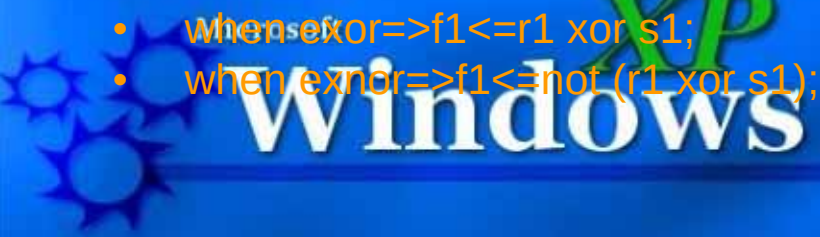
- ALU.vhd由微指令控制，实现由操作数多路选择器送来的r和s的4位数据进行加、减、或、与、与非、异或、异或非等算术和逻辑运算；

- Port (
r : --由SRC_OP输出的信号r
s : --由SRC_OP输出的信号r
c_n : --进位输入
alu_ct1 : --alu控制
f : --输出数据
g_bar : --预置进位
p_bar : --进位传输
c_n4 : --进位标志输出
ovr : --溢出

ALU. vhd

```
when add =>
        if c_n='0' then
        F1<=r1+s1;          --向量加法
        else
        F1<=r1+s1+1;
        End if;
when subr =>
        if c_n='0' then
        F1<=r1+not(s1)+1;       --补码
        else
        F1<=r1+not(s1);
        End if;
when orrs=>f1<=r1 or s1;
when andrs=>f1<=r1 and s1;
when notrs=>f1<=not r1 and s1;
when exor=>f1<=r1 xor s1;
when exnor=>f1<=not (r1 xor s1);
```

- use IEEE.STD_LOGIC_1164.ALL;--逻辑运算
- use ieee.numeric_std.all; –数字运算
- use IEEE.STD_LOGIC_UNSIGNED.ALL; ;--向量运算、赋值



ALU. vhd

- F <= f1(3 downto 0); -- outside the process
- C_n4 <= f1(4);
- G_bar <= not ((r(3) and s(3)) or ((r(3) or s(3)) and (r(2) and s(2))) or ((r(3) or s(3)) and (r(2) or s(2)) and(r(1)and s(1))) or((r(3) or s(3)) and (r(2) or s(2)) and (r(1) or(1)) and(r(0) and s(0))));
- p_bar <=not ((r(3) or s(3)) and (r(2) or s(2)) and (r(1) and s(1)) and(r(0) and s(0)));
- ovr <= (f1(4)xor f1(3));

- 等价：
- G_bar=~(R3*S3+(R3+S3)R2*S2+
- (R3+S3)(R2+S2)R1*S1+(R3+S3)(R2+S2)(R1+S1)R0*S0)
- P_bar=~((R3+S3)(R2+S2)*R1*R0*S1*S0)
- OVR='1' WHEN (f(4)/=f(3)) else
- '0'

SRC_OP.vhd

- SRC_OP.vhd操作数多路选择器由两个多路选择器组成，分别由微指令控制r,s输出的4位输入数据，输出输入对应关系如下：
- r:输入数据d（外围4位数据）、ad（ram的数据），GND
- s:输入数据q（Q_REG中数据）、ad（ram的数据）,bd（ram的另一组数据）,GND

```
--define alu operand r:
with src_ctl select
        r <= ad when aq|ab,
                "0000"when zq|zb|za,
                d when others;

--r input
with src_ctl select
        s <=q when aq|zq|dq,
                bd when ab|zb,
                ad when za|da,
                "0000" when others;

--s
```

RAM_REGS.vhd

- RAM　16 BYTES
- 可移位

- 寄存器建立：

- gen: for i in 15 downto 0
- 　generate
- 　　ram: ureg generic map (4)
- 　　port map (clk, rst, en(i), data, ab_data(i));
- end generate;

- 移位实现：
- With dest_ctl select
- data <=(f(2),f(1),f(0),ram0) when ramqu |ramu,
  (ram3,f(3),f(2),f(1)) when ramqd|ramd,
  "----" when others;
- ad <= ab_data(conv_integer(a));
- bd <= ab_data(conv_integer(b)); ;
- ram3 <=f(3) when (dest_ctl= ramu or dest_ctl=ramqu) else 'Z';
- ram0 <=f(0) when (dest_ctl= ramu or dest_ctl=ramqu) else 'Z';

cpu_4comps.vhd

- Package cpu_4comps is
- ……..
- End cpu_4comps;

am2901.vhd

```
u1:ram_regs port map(clk=>clk,rst=>rst,a=>a,b=>b,f=>f,
        dest_ctl=>dest_ctl,ram0=>ram0,ram3=>ram3,ad=>ad,bd=>bd);
    u2:q_reg port map (clk=>clk,rst=>rst,f=>f,dest_ctl=>dest_ctl,
        qs0=>qs0,qs3=>qs3,q=>q);
    u3:src_op port map(d=>d,ad=>ad,bd=>bd,q=>q,src_ctl=>src_ctl,
        r=>r,s=>s);
    u4:alu port map (r=>r,s=>s,c_n=>c_n,alu_ct1 =>alu_ct1 ,f=>f,
        g_bar=>g_bar,p_bar=>p_bar,c_n4=>c_n4,ovr=>ovr);
    u5:out_mux port map (ad=>ad, f=>f, dest_ctl=>dest_ctl,oe=>oe,y=>y);


    f_0 <='0' when f="0000"else 'Z';
    f3<=f(3);
```

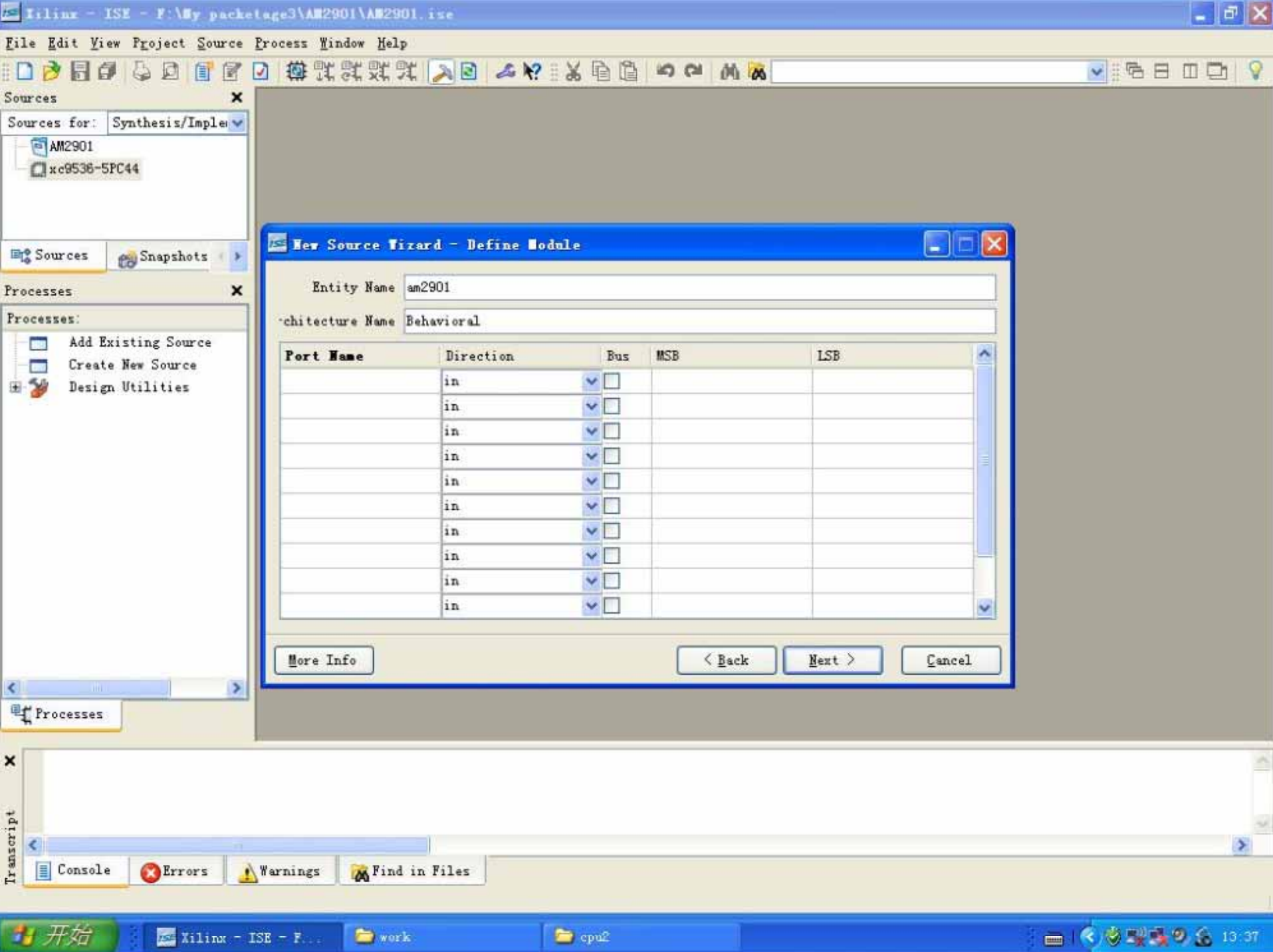
系统实现

开发软件： Xilinx ISE

Xilinx ISE为Xilinx公司开发的可编程逻辑器件的开发环境。Xlinx为全球最大的可编程逻辑器件开发商之一，在FPGA领域起更是处于独领风骚的地位。其开发的这款软件最好可以由ModelSim仿真软件辅助仿真。

Xilinx ISE

设置


Xilinx - ISE - F:\My packetage3\AM2901\AM2901.ise
File Edit View Project Source Process Window Help
Sources
Sources for: Synthesis/Imple
AM2901
xc9536-5PC44
Sources
Snapshots
Processes
Processes:
Add Existing Source
Create New Source
Design Utilities
Processes
New Source Wizard - Define Module
Entity Name am2901
chitecture Name Behavioral
Port Name
Direction
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More Info
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Transcript
Console
Errors
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Find in Files
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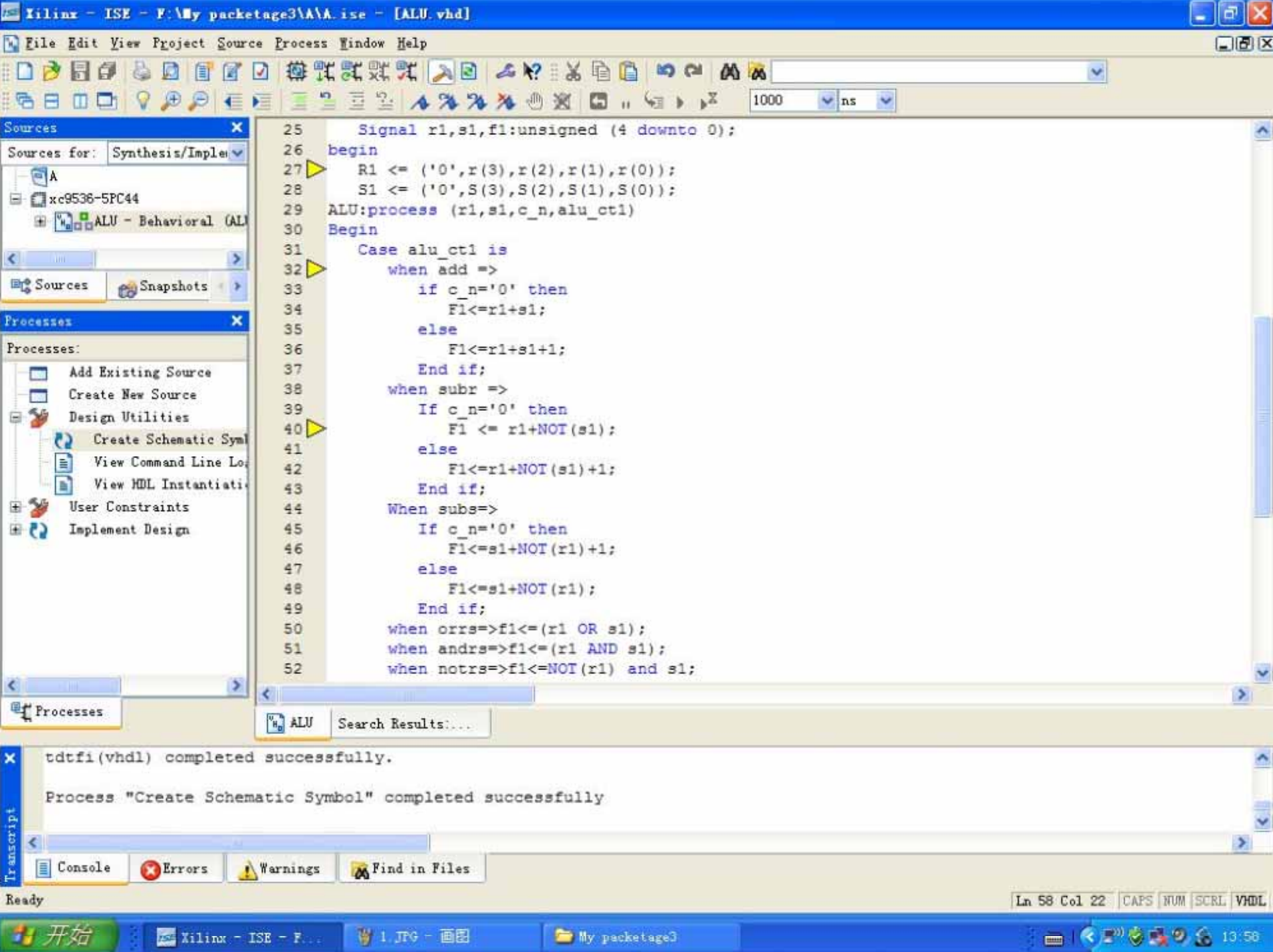
Xilinx - ISE - F...
work
cpu2
13:37

编译过程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Design Utilities
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Implement Design
Processes
25 Signal r1,s1,f1:unsigned (4 downto 0);
26 begin
27 R1 <= ('0',r(3),r(2),r(1),r(0));
28 S1 <= ('0',S(3),S(2),S(1),S(0));
29 ALU:process (r1,s1,c_n,alu_ct1)
30 Begin
31 Case alu_ct1 is
32 when add =>
33 if c_n='0' then
34 F1<=r1+s1;
35 else
36 F1<=r1+s1+1;
37 End if;
38 when subr =>
39 If c_n='0' then
40 F1 <= r1+NOT(s1);
41 else
42 F1<=r1+NOT(s1)+1;
43 End if;
44 When subs=>
45 If c_n='0' then
46 F1<=s1+NOT(r1)+1;
47 else
48 F1<=s1+NOT(r1);
49 End if;
50 when orrs=>f1<=(r1 OR s1);
51 when andrs=>f1<=(r1 AND s1);
52 when notrs=>f1<=NOT(r1) and s1;
ALU
Search Results:...
tdtfi(vhdl) completed successfully.
Process "Create Schematic Symbol" completed successfully
Transcript
Console
Errors
Warnings
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CAPS NUM SCRL VHDL
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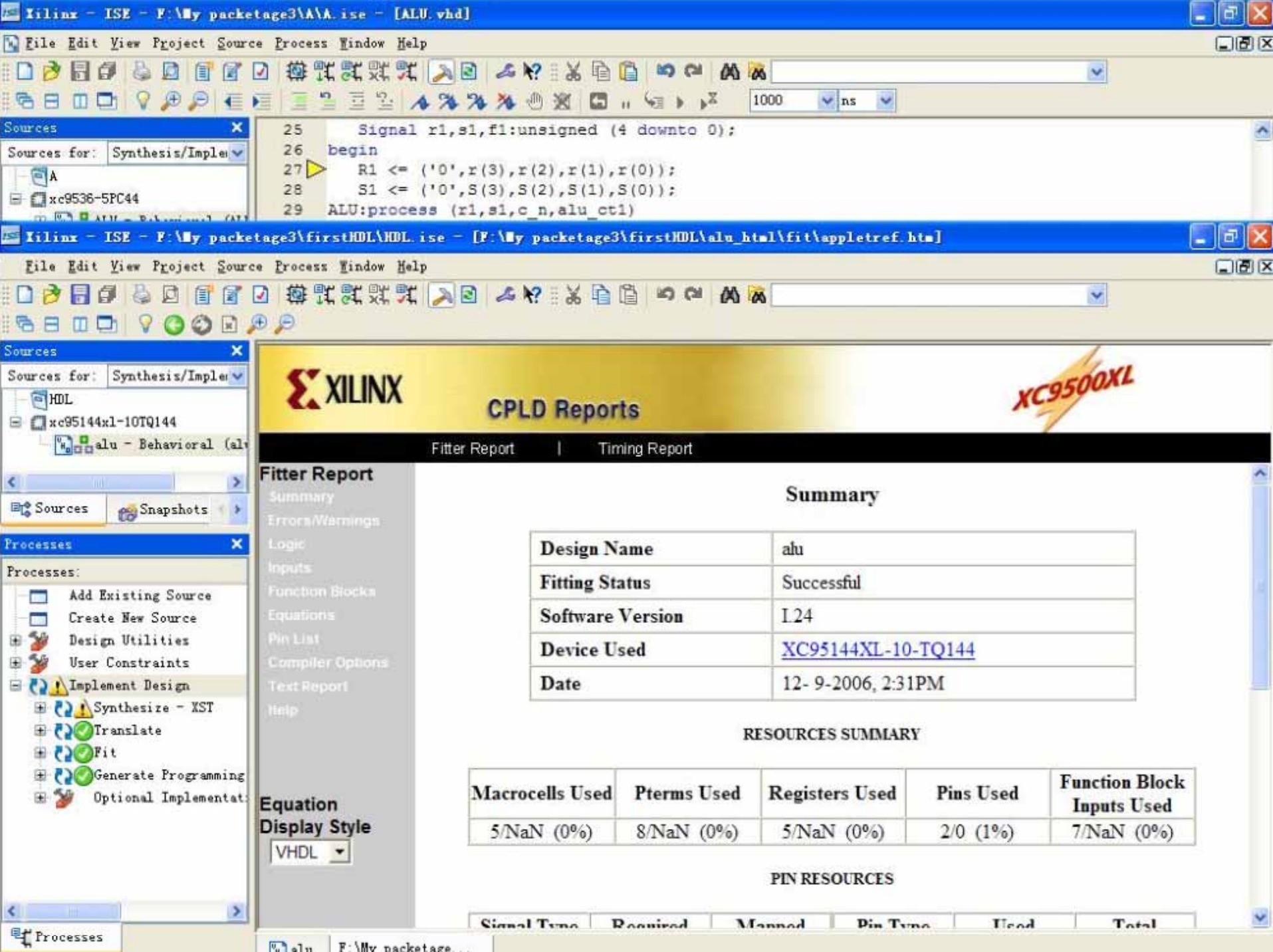
Xilinx - ISE - F...
1.JPG - 画图
My packetage3
13:58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25 Signal r1,s1,f1:unsigned (4 downto 0);
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Create New Source
Design Utilities
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Implement Design
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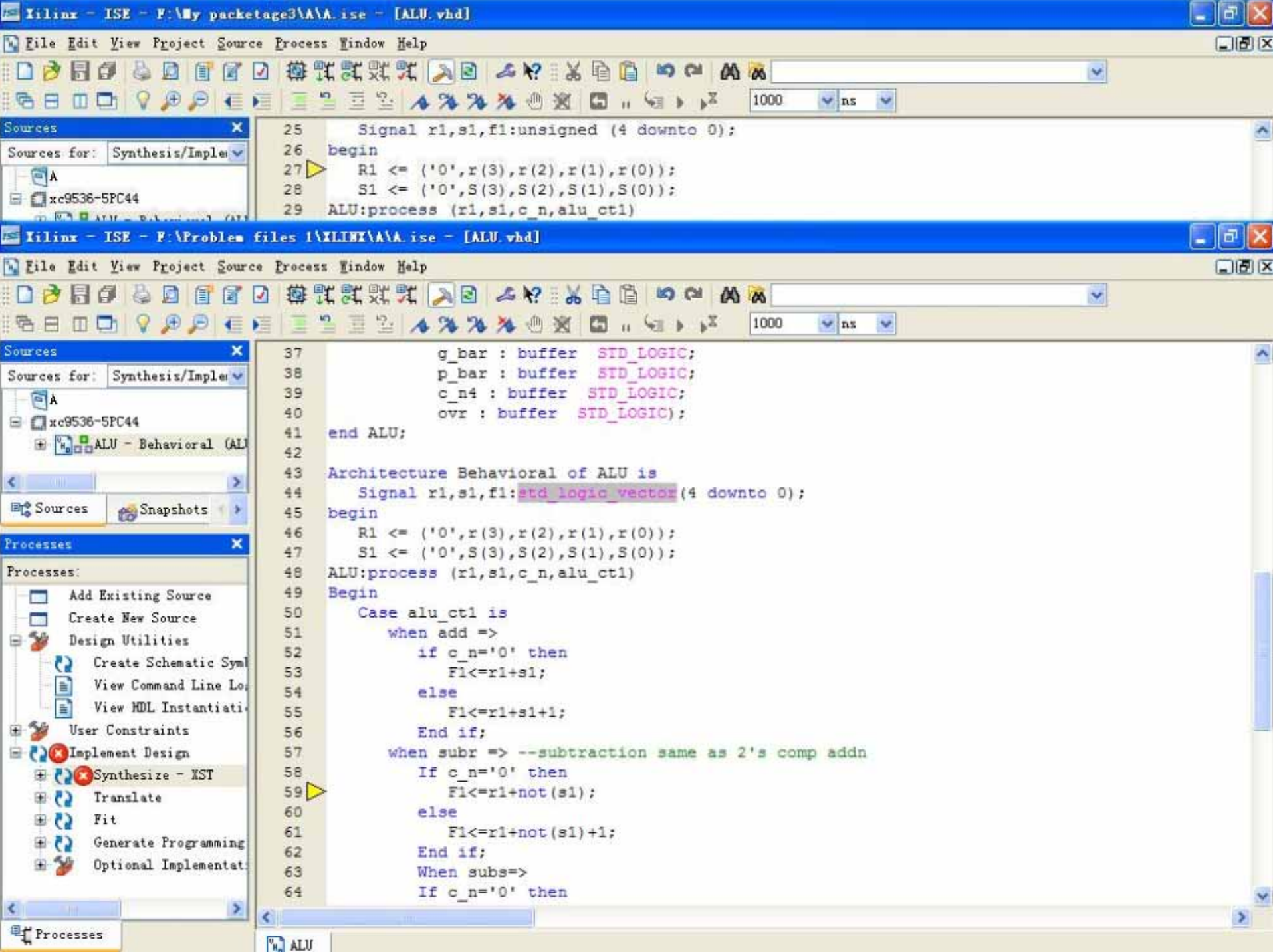
Summary
Errors/Warnings
Logic
Inputs
Function Blocks
Equations
Pin List
Compiler Options
Text Report
Help
Equation Display Style
VHDL
Summary
Design Name alu
Fitting Status Successful
Software Version I.24
Device Used XC95144XL-10-TQ144
Date 12- 9-2006, 2:31PM
RESOURCES SUMMARY
Macrocells Used Pterms Used Registers Used Pins Used Function Block Inputs Used
5/NaN (0%) 8/NaN (0%) 5/NaN (0%) 2/0 (1%) 7/NaN (0%)
PIN RESOURCES
Signal Type Required Mapped Pin Type Used Total
alu F:\My packetage...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File Edit View Project Source Process Window Help
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A
xc9536-5PC44
25 Signal r1,s1,f1:unsigned (4 downto 0);
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28 S1 <= ('0',S(3),S(2),S(1),S(0));
29 ALU:process (r1,s1,c_n,alu_ct1)
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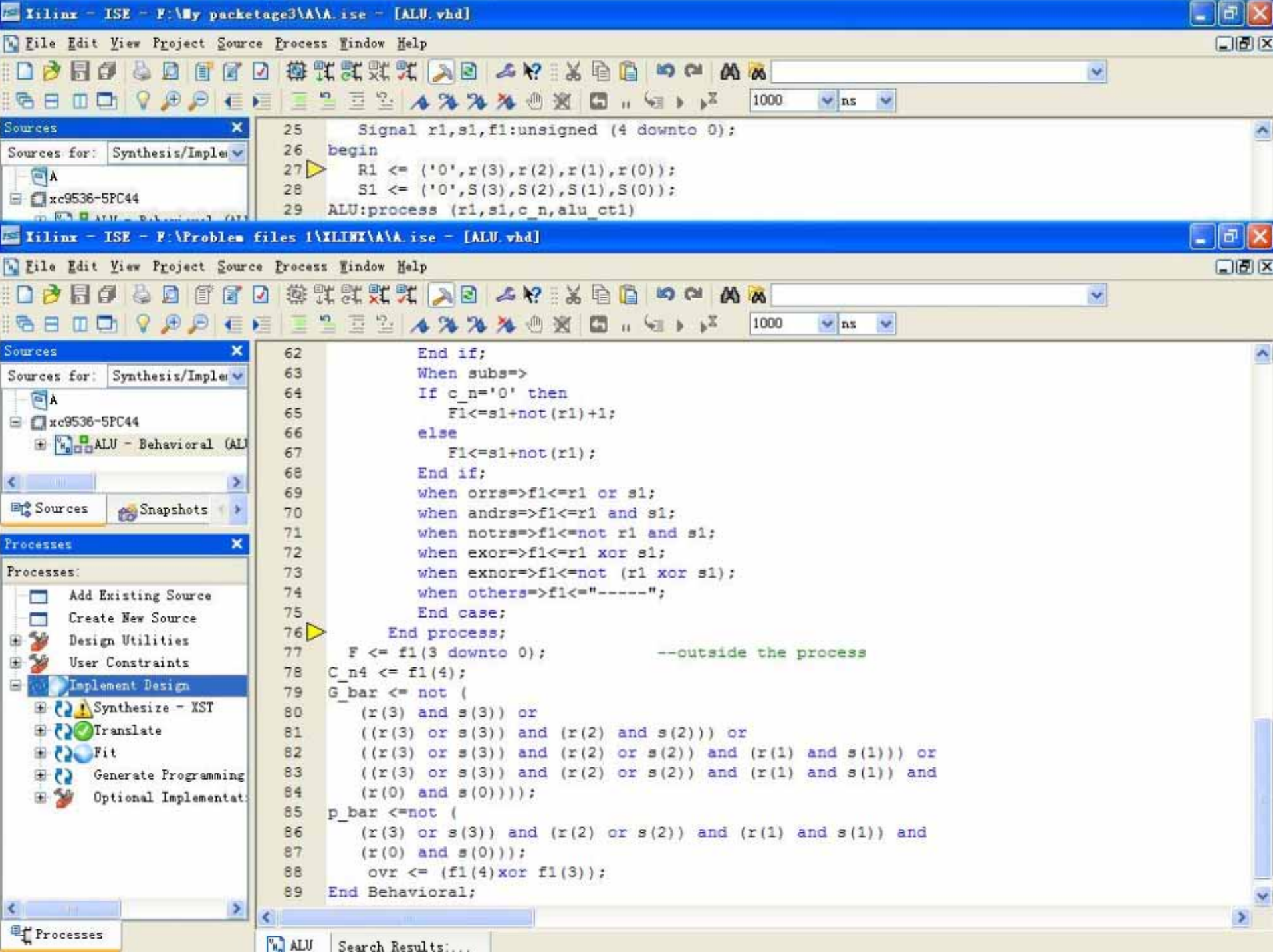
Design Utilities
Create Schematic Symbol
View Command Line Log
View HDL Instantiation
User Constraints
Implement Design
Synthesize - XST
Translate
Fit
Generate Programming
Optional Implementat
Processes
37 g_bar : buffer STD_LOGIC;
38 p_bar : buffer STD_LOGIC;
39 c_n4 : buffer STD_LOGIC;
40 ovr : buffer STD_LOGIC);
41 end ALU;
42
43 Architecture Behavioral of ALU is
44 Signal r1,s1,f1:std_logic_vector(4 downto 0);
45 begin
46 R1 <= ('0',r(3),r(2),r(1),r(0));
47 S1 <= ('0',S(3),S(2),S(1),S(0));
48 ALU:process (r1,s1,c_n,alu_ct1)
49 Begin
50 Case alu_ct1 is
51 when add =>
52 if c_n='0' then
53 F1<=r1+s1;
54 else
55 F1<=r1+s1+1;
56 End if;
57 when subr => --subtraction same as 2's comp addn
58 If c_n='0' then
59 F1<=r1+not(s1);
60 else
61 F1<=r1+not(s1)+1;
62 End if;
63 When subs=>
64 If c_n='0' then
ALU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xc9536-5PC44
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29 ALU:process (r1,s1,c_n,alu_ct1)
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Create New Source
Design Utilities
User Constraints
Implement Design
Synthesize - XST
Translate
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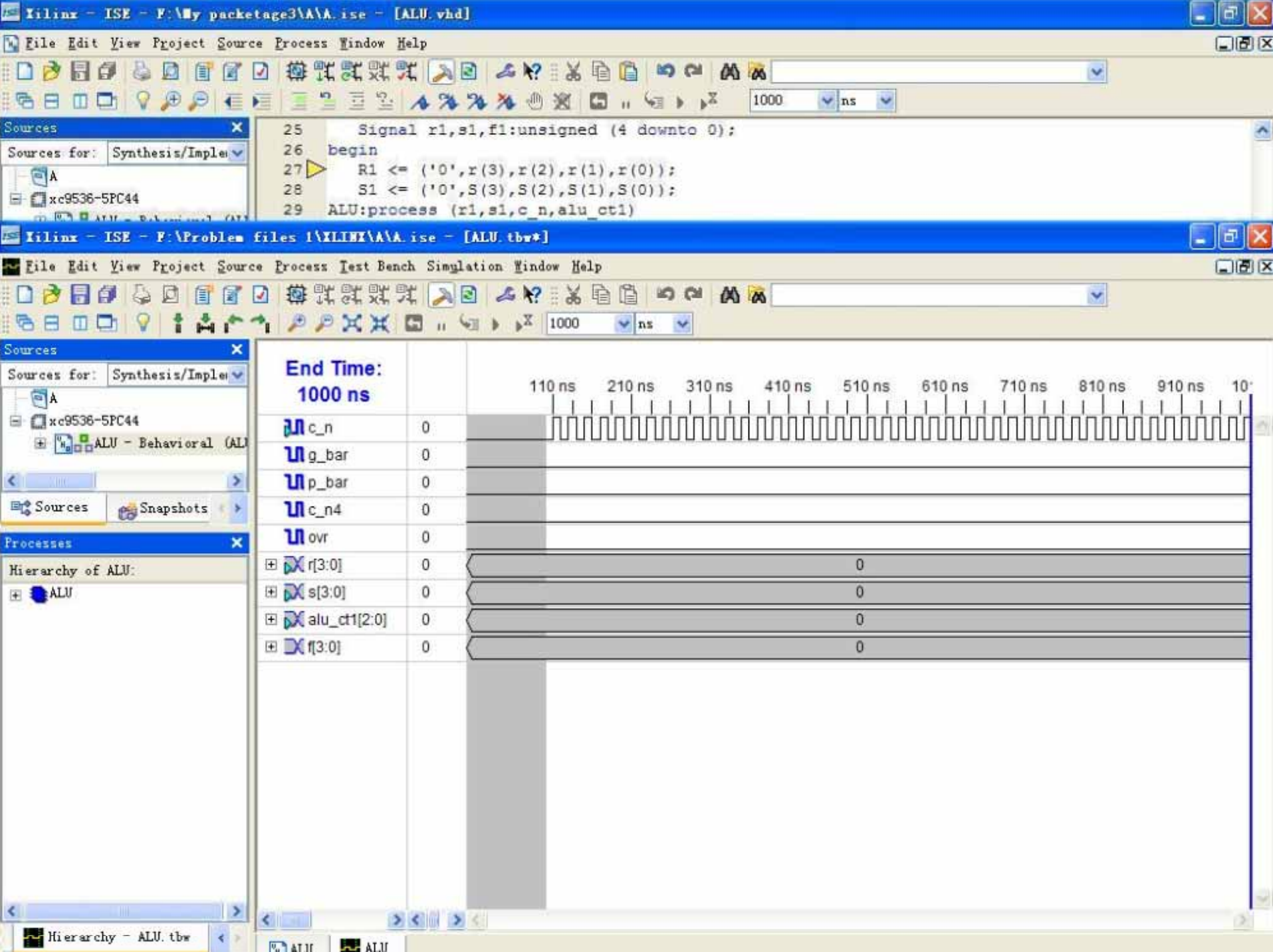
Generate Programming
Optional Implementat
Processes
62 End if;
63 When subs=>
64 If c_n='0' then
65 F1<=s1+not(r1)+1;
66 else
67 F1<=s1+not(r1);
68 End if;
69 when orrs=>f1<=r1 or s1;
70 when andrs=>f1<=r1 and s1;
71 when notrs=>f1<=not r1 and s1;
72 when exor=>f1<=r1 xor s1;
73 when exnor=>f1<=not (r1 xor s1);
74 when others=>f1<="-----";
75 End case;
76 End process;
77 F <= f1(3 downto 0); --outside the process
78 C_n4 <= f1(4);
79 G_bar <= not (
80 (r(3) and s(3)) or
81 ((r(3) or s(3)) and (r(2) and s(2))) or
82 ((r(3) or s(3)) and (r(2) or s(2)) and (r(1) and s(1))) or
83 ((r(3) or s(3)) and (r(2) or s(2)) and (r(1) and s(1)) and
84 (r(0) and s(0))));
85 p_bar <=not (
86 (r(3) or s(3)) and (r(2) or s(2)) and (r(1) and s(1)) and
87 (r(0) and s(0)));
88 ovr <= (f1(4)xor f1(3));
89 End Behavioral;
ALU
Search Results:...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25 Signal r1,s1,f1:unsigned (4 downto 0);
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28 S1 <= ('0',S(3),S(2),S(1),S(0));
29 ALU:process (r1,s1,c_n,alu_ct1)
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File Edit View Project Source Process Test Bench Simulation Window Help
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ALU - Behavioral (ALU
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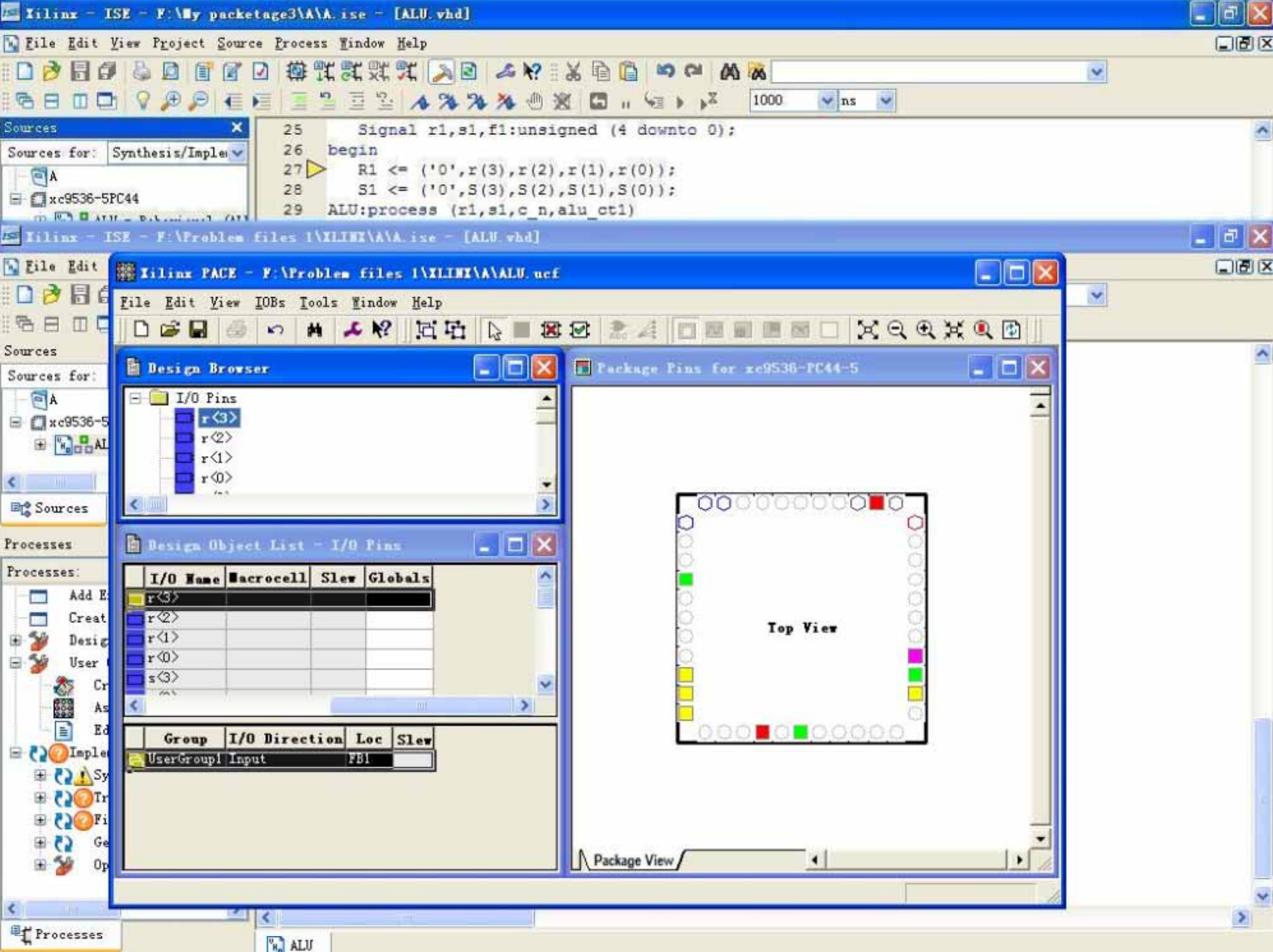
Snapshots
Processes
Hierarchy of ALU:
ALU
Hierarchy - ALU.tbw
End Time:
1000 ns
110 ns
210 ns
310 ns
410 ns
510 ns
610 ns
710 ns
810 ns
910 ns
c_n 0
g_bar 0
p_bar 0
c_n4 0
ovr 0
r[3:0] 0 0
s[3:0] 0 0
alu_ct1[2:0] 0 0
f[3:0] 0 0
ALU
ALU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29 ALU:process (r1,s1,c_n,alu_ct1)
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Xilinx PACE - F:\Problem files 1\XLINX\A\ALU.ucf
File Edit View IOBs Tools Window Help
Design Browser
I/O Pins
r<3>
r<2>
r<1>
r<0>
Design Object List - I/O Pins
I/O Name Macrocell Slew Globals
r<3>
r<2>
r<1>
r<0>
s<3>
Group I/O Direction Loc Slew
UserGroup1 Input P81
Package Pins for xc9536-PC44-5
Top View
Package View
Sources
Processes
Add E
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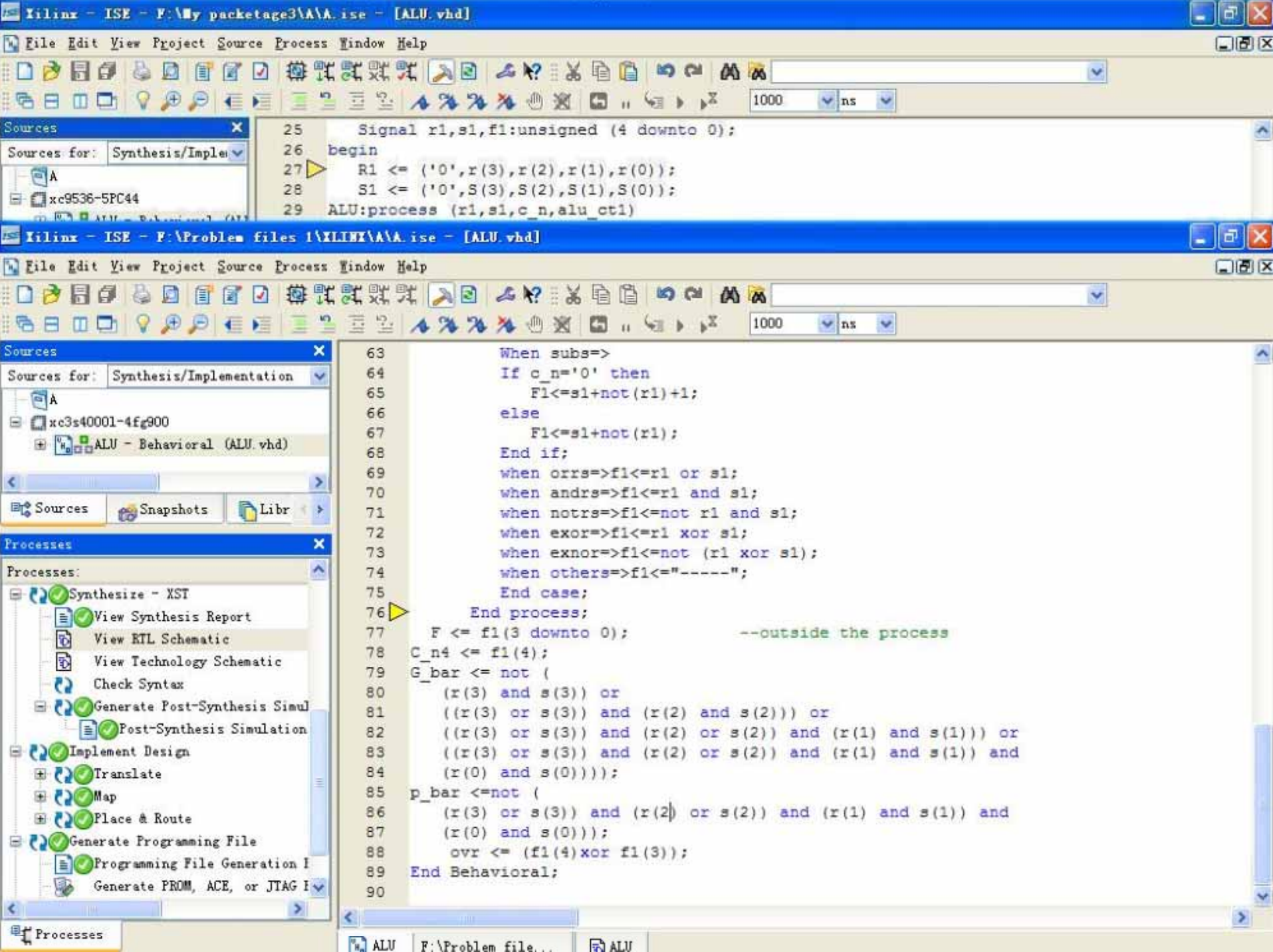
ALU


Xilinx - ISE - F:\My packetage3\A\A.ise - [ALU.vhd]
File Edit View Project Source Process Window Help
Sources
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A
xc9536-5PC44
25 Signal r1,s1,f1:unsigned (4 downto 0);
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27 R1 <= ('0',r(3),r(2),r(1),r(0));
28 S1 <= ('0',S(3),S(2),S(1),S(0));
29 ALU:process (r1,s1,c_n,alu_ct1)
Xilinx - ISE - F:\Problem files 1\XILINX\A\A.ise - [ALU.vhd]
File Edit View Project Source Process Window Help
1000 ns
Sources
Sources for: Synthesis/Implementation
A
xc3s400l-4fg900
ALU - Behavioral (ALU.vhd)
Sources Snapshots Libr
Processes
Processes:
Synthesize - XST
View Synthesis Report
View RTL Schematic
View Technology Schematic
Check Syntax
Generate Post-Synthesis Simul
Post-Synthesis Simulation
Implement Design
Translate
Map
Place & Route
Generate Programming File
Programming File Generation I
Generate PROM, ACE, or JTAG I
Processes
63 When subs=>
64 If c_n='0' then
65 F1<=s1+not(r1)+1;
66 else
67 F1<=s1+not(r1);
68 End if;
69 when orrs=>f1<=r1 or s1;
70 when andrs=>f1<=r1 and s1;
71 when notrs=>f1<=not r1 and s1;
72 when exor=>f1<=r1 xor s1;
73 when exnor=>f1<=not (r1 xor s1);
74 when others=>f1<="-----";
75 End case;
76 End process;
77 F <= f1(3 downto 0); --outside the process
78 C_n4 <= f1(4);
79 G_bar <= not (
80 (r(3) and s(3)) or
81 ((r(3) or s(3)) and (r(2) and s(2))) or
82 ((r(3) or s(3)) and (r(2) or s(2)) and (r(1) and s(1))) or
83 ((r(3) or s(3)) and (r(2) or s(2)) and (r(1) and s(1)) and
84 (r(0) and s(0))));
85 p_bar <=not (
86 (r(3) or s(3)) and (r(2) or s(2)) and (r(1) and s(1)) and
87 (r(0) and s(0)));
88 ovr <= (f1(4)xor f1(3));
89 End Behavioral;
90
ALU F:\Problem file... ALU

Xilinx - ISE - F:\My packetage3\A\A.ise - [ALU.vhd]

File Edit View Project Source Process Window Help

Sources

Sources for: Synthesis/Imple

A

xc9536-5PC44

```
25    Signal r1,s1,f1:unsigned (4 downto 0);
26  begin
27    R1 <= ('0',r(3),r(2),r(1),r(0));
28    S1 <= ('0',S(3),S(2),S(1),S(0));
29  ALU:process (r1,s1,c_n,alu_ct1)
```

Xilinx - ISE - F:\Problem files 1\XILINX\A\A.ise - [ALU.ngr]

File Edit View Project Source Process Window Help

Sources

ALU

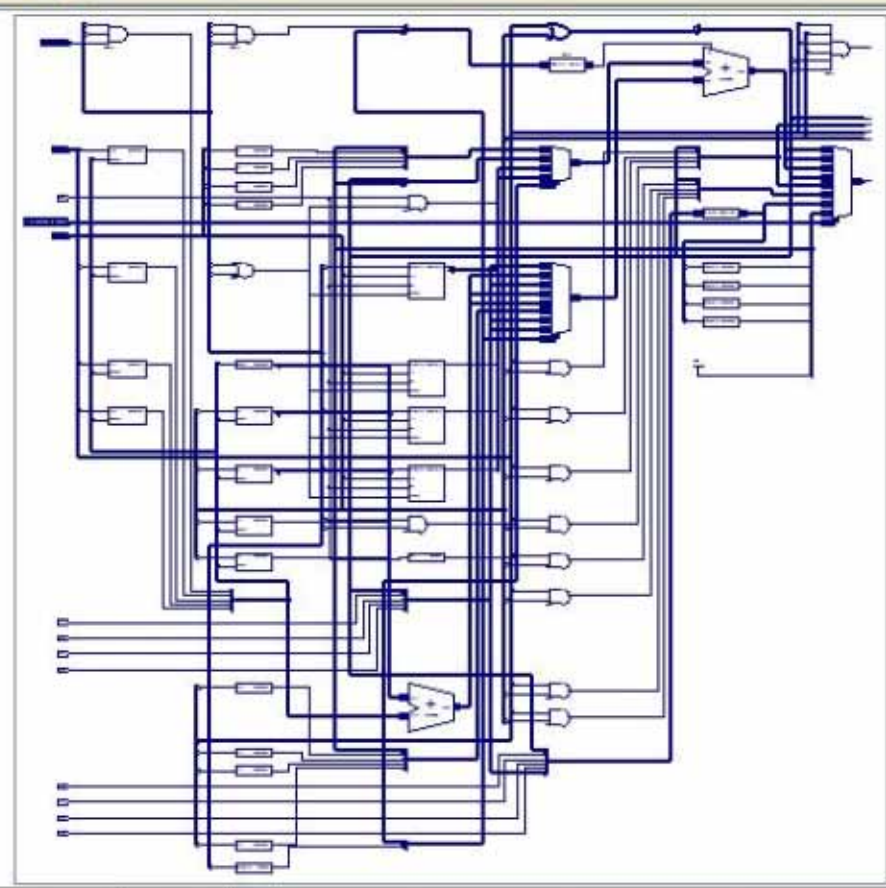
- _n0006<0>_imp
- _n0006<1>_imp
- _n0006<2>_imp
- _n0006<3>_imp
- _n0007<0>_imp
- _n0007<1>_imp
- _n0007<2>_imp
- _n0007<3>_imp

Snapshots Libraries Design

Processes

No flow available.

Processes



ALU F:\Problem file... ALU

Xilinx - ISE - F:\My packetage3\A\A.ise - [ALU.vhd]

File Edit View Project Source Process Window Help

Sources

Sources for: Synthesis/Imple

A

xc9536-5PC44

```
25    Signal r1,s1,f1:unsigned (4 downto 0);
26  begin
27    R1 <= ('0',r(3),r(2),r(1),r(0));
28    S1 <= ('0',S(3),S(2),S(1),S(0));
29  ALU:process (r1,s1,c_n,alu_ct1)
```

Xilinx - ISE - F:\Problem files 1\XILINX\A\A.ise - [ALU.ngc]

File Edit View Project Source Process Window Help

Sources

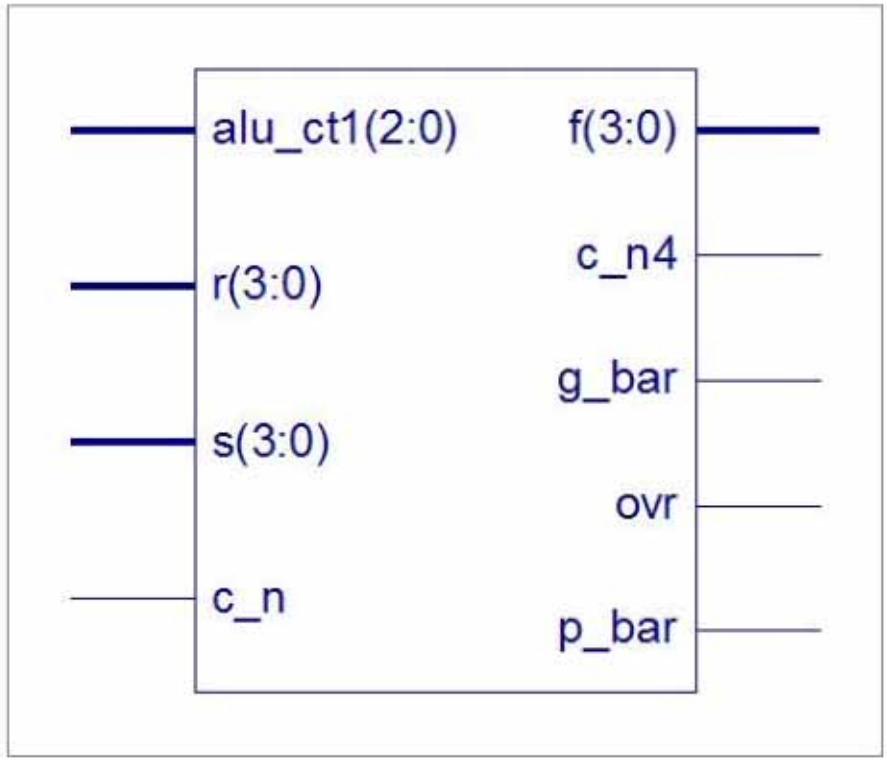
ALU

Snapshots Libraries Design

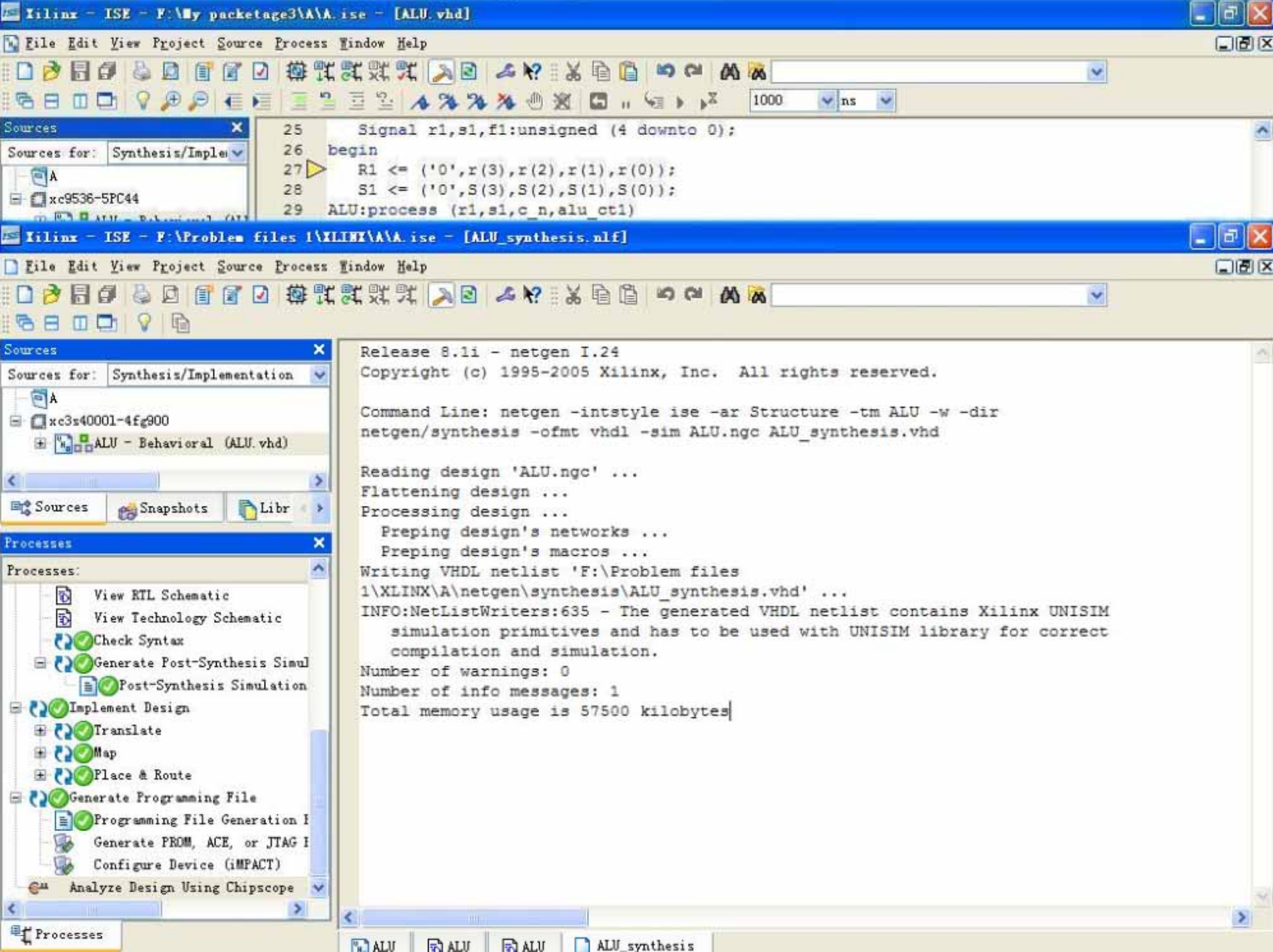
Processes

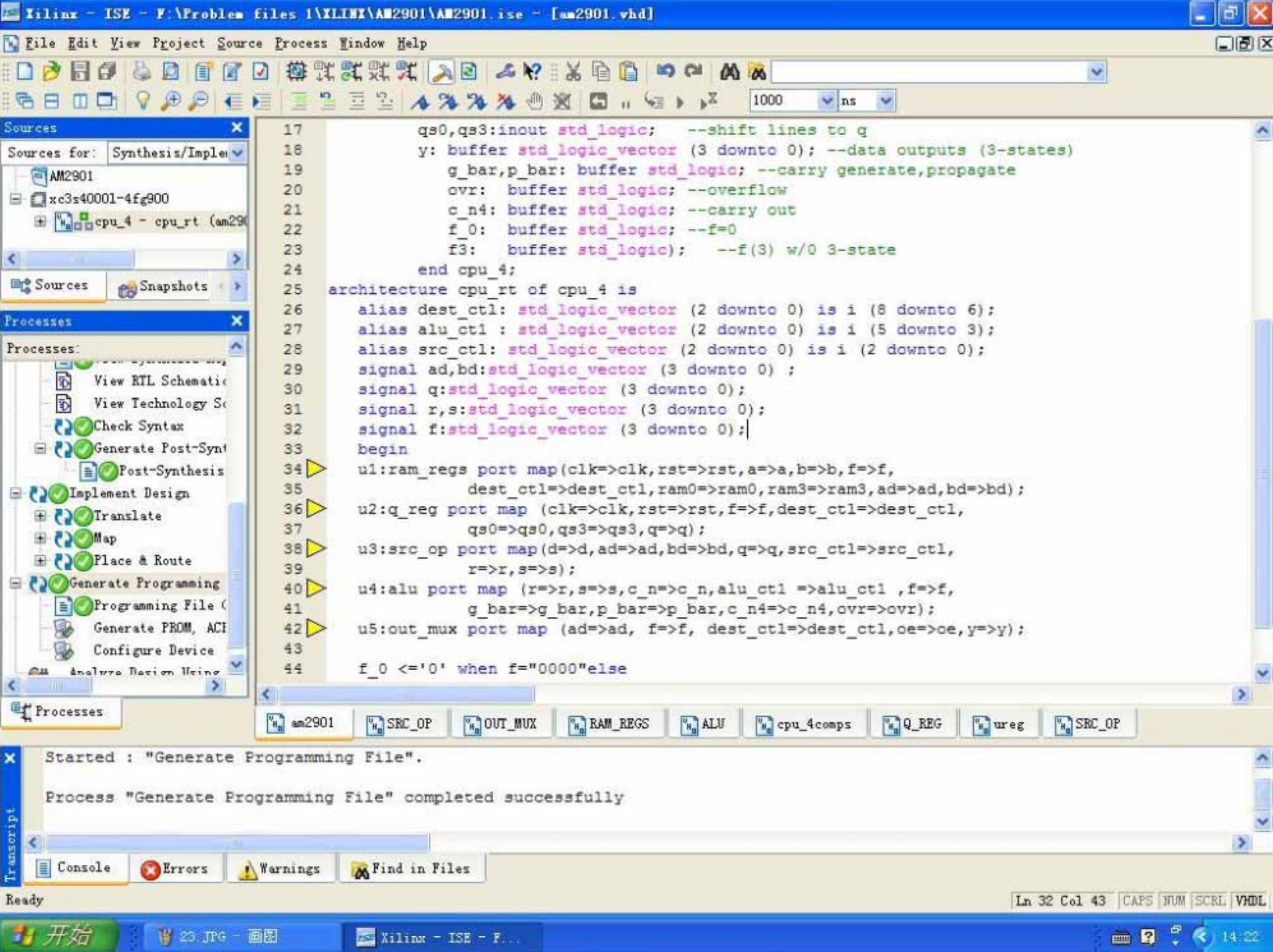
No flow available.

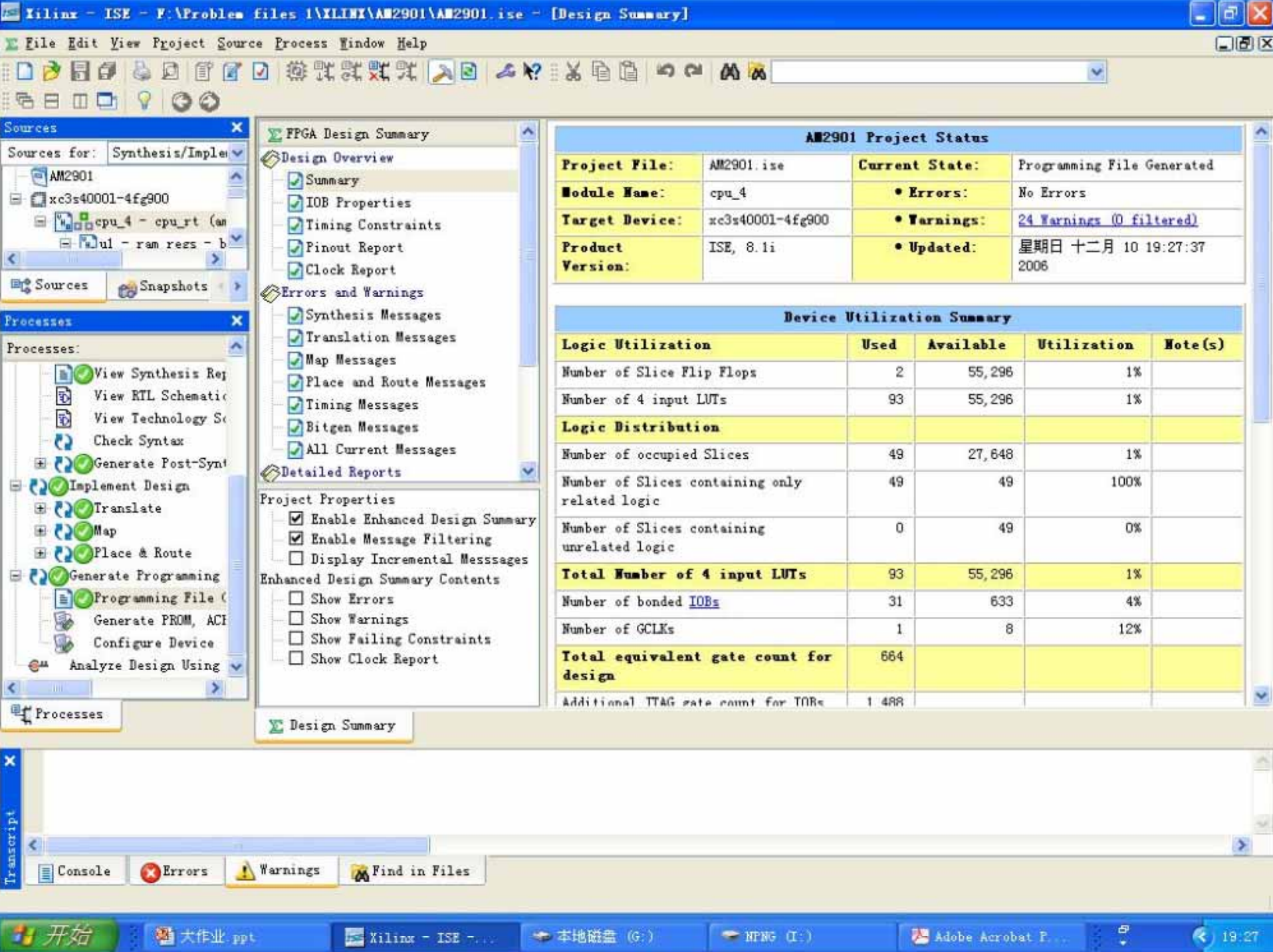
Processes



ALU F:\Problem file... ALU ALU


Xilinx - ISE - F:\My packetage3\A\A.ise - [ALU.vhd]
File Edit View Project Source Process Window Help
Sources
Sources for: Synthesis/Imple
A
xc9536-5PC44
25 Signal r1,s1,f1:unsigned (4 downto 0);
26 begin
27 R1 <= ('0',r(3),r(2),r(1),r(0));
28 S1 <= ('0',S(3),S(2),S(1),S(0));
29 ALU:process (r1,s1,c_n,alu_ct1)
Xilinx - ISE - F:\Problem files 1\XLINX\A\A.ise - [ALU_synthesis.nlf]
File Edit View Project Source Process Window Help
Sources
Sources for: Synthesis/Implementation
A
xc3s400l-4fg900
ALU - Behavioral (ALU.vhd)
Sources
Snapshots
Libr
Processes
Processes:
View RTL Schematic
View Technology Schematic
Check Syntax
Generate Post-Synthesis Simul
Post-Synthesis Simulation
Implement Design
Translate
Map
Place & Route
Generate Programming File
Programming File Generation I
Generate PROM, ACE, or JTAG I
Configure Device (iMPACT)
Analyze Design Using Chipscope
Release 8.1i - netgen I.24
Copyright (c) 1995-2005 Xilinx, Inc. All rights reserved.
Command Line: netgen -intstyle ise -ar Structure -tm ALU -w -dir
netgen/synthesis -ofmt vhdl -sim ALU.ngc ALU_synthesis.vhd
Reading design 'ALU.ngc' ...
Flattening design ...
Processing design ...
Preping design's networks ...
Preping design's macros ...
Writing VHDL netlist 'F:\Problem files
1\XLINX\A\netgen\synthesis\ALU_synthesis.vhd' ...
INFO:NetListWriters:635 - The generated VHDL netlist contains Xilinx UNISIM
simulation primitives and has to be used with UNISIM library for correct
compilation and simulation.
Number of warnings: 0
Number of info messages: 1
Total memory usage is 57500 kilobytes
Processes
ALU
ALU
ALU
ALU_synthesis


Xilinx - ISE - F:\Problem files 1\XILINX\AM2901\AM2901.ise - [am2901.vhd]
File Edit View Project Source Process Window Help
Sources
Sources for: Synthesis/Imple
AM2901
xc3s400l-4fg900
cpu_4 - cpu_rt (am29
Sources
Snapshots
Processes
Processes:
View RTL Schematic
View Technology Sc
Check Syntax
Generate Post-Synt
Post-Synthesis
Implement Design
Translate
Map
Place & Route
Generate Programming
Programming File (
Generate PROM, ACE
Configure Device
Processes
17 qs0,qs3:inout std_logic; --shift lines to q
18 y: buffer std_logic_vector (3 downto 0); --data outputs (3-states)
19 g_bar,p_bar: buffer std_logic; --carry generate,propagate
20 ovr: buffer std_logic; --overflow
21 c_n4: buffer std_logic; --carry out
22 f_0: buffer std_logic; --f=0
23 f3: buffer std_logic); --f(3) w/0 3-state
24 end cpu_4;
25 architecture cpu_rt of cpu_4 is
26 alias dest_ctl: std_logic_vector (2 downto 0) is i (8 downto 6);
27 alias alu_ctl : std_logic_vector (2 downto 0) is i (5 downto 3);
28 alias src_ctl: std_logic_vector (2 downto 0) is i (2 downto 0);
29 signal ad,bd:std_logic_vector (3 downto 0) ;
30 signal q:std_logic_vector (3 downto 0);
31 signal r,s:std_logic_vector (3 downto 0);
32 signal f:std_logic_vector (3 downto 0);
33 begin
34 u1:ram_regs port map(clk=>clk,rst=>rst,a=>a,b=>b,f=>f,
35 dest_ctl=>dest_ctl,ram0=>ram0,ram3=>ram3,ad=>ad,bd=>bd);
36 u2:q_reg port map (clk=>clk,rst=>rst,f=>f,dest_ctl=>dest_ctl,
37 qs0=>qs0,qs3=>qs3,q=>q);
38 u3:src_op port map(d=>d,ad=>ad,bd=>bd,q=>q,src_ctl=>src_ctl,
39 r=>r,s=>s);
40 u4:alu port map (r=>r,s=>s,c_n=>c_n,alu_ctl =>alu_ctl ,f=>f,
41 g_bar=>g_bar,p_bar=>p_bar,c_n4=>c_n4,ovr=>ovr);
42 u5:out_mux port map (ad=>ad, f=>f, dest_ctl=>dest_ctl,oe=>oe,y=>y);
43
44 f_0 <='0' when f="0000"else
1000 ns
am2901
SRC_OP
OUT_MUX
RAM_REGS
ALU
cpu_4comps
Q_REG
ureg
SRC_OP
Started : "Generate Programming File".
Process "Generate Programming File" completed successfully
Transcript
Console
Errors
Warnings
Find in Files
Ready
Ln 32 Col 43
CAPS NUM SCRL VHDL
开始
23.JPG - 画图
Xilinx - ISE - F...
14:22


Xilinx - ISE - F:\Problem files 1\XILINX\AM2901\AM2901.ise - [Design Summary]
File Edit View Project Source Process Window Help
Sources
Sources for: Synthesis/Imple
AM2901
xc3s40001-4fg900
cpu_4 - cpu_rt (an
u1 - ram regs - b
Sources
Snapshots
Processes
Processes:
View Synthesis Rep
View RTL Schematic
View Technology Sc
Check Syntax
Generate Post-Synt
Implement Design
Translate
Map
Place & Route
Generate Programming
Programming File (
Generate PROM, ACE
Configure Device
Analyze Design Using
Processes
FPGA Design Summary
Design Overview
Summary
IOB Properties
Timing Constraints
Pinout Report
Clock Report
Errors and Warnings
Synthesis Messages
Translation Messages
Map Messages
Place and Route Messages
Timing Messages
Bitgen Messages
All Current Messages
Detailed Reports
Project Properties
Enable Enhanced Design Summary
Enable Message Filtering
Display Incremental Messsages
Enhanced Design Summary Contents
Show Errors
Show Warnings
Show Failing Constraints
Show Clock Report
Design Summary
AM2901 Project Status
Project File: AM2901.ise
Current State: Programming File Generated
Module Name: cpu_4
• Errors: No Errors
Target Device: xc3s40001-4fg900
• Warnings: 24 Warnings (0 filtered)
Product Version: ISE, 8.1i
• Updated: 星期日 十二月 10 19:27:37 2006
Device Utilization Summary
Logic Utilization | Used | Available | Utilization | Note(s)
Number of Slice Flip Flops | 2 | 55,296 | 1%
Number of 4 input LUTs | 93 | 55,296 | 1%
Logic Distribution
Number of occupied Slices | 49 | 27,648 | 1%
Number of Slices containing only related logic | 49 | 49 | 100%
Number of Slices containing unrelated logic | 0 | 49 | 0%
Total Number of 4 input LUTs | 93 | 55,296 | 1%
Number of bonded IOBs | 31 | 633 | 4%
Number of GCLKs | 1 | 8 | 12%
Total equivalent gate count for design | 664
Additional JTAG gate count for IOBs | 1,488
Transcript
Console
Errors
Warnings
Find in Files
开始
大作业.ppt
Xilinx - ISE -...
本地磁盘 (G:)
NPNG (I:)
Adobe Acrobat P...
19:27

微指令标

- ALU操作数选择指令

aq ab zq zb za da dq dz

- ALU 算术与逻辑指令

add subr subs orrs andrs notrs exor exnor

- ALU 寄存器输入输出移位指令

qreg nop rama ramf ramqd ramd ramqu ramu

- The end

Basic 元件包

- regs_pkg.vhd为打包的顶层元件包的描述，其余分别对应着一种较为基本的数字元件；
- rdff.vhd
- rdff1.vhd
- rreg1.vhd
- rreg.vhd
- reg.vhd ascount.vhd
- rsynch.vhd和psynch.vhd
- ureg.vhd

返回

Work程序包

- cpu_4comps.vhd为顶层元件包描述，其余对应着AM2901的某一构成部分：
- OUT_MUX.vhd
- ALU.vhd
- SRC_OP.vhd
- ram_regs.vhd
- Q_REG.vhd
- 此外，mnemonics.vhd为微控制指令代码程序。

返回